REMARKS

This amendment is responsive to the Final Office Action dated May 31, 2005. Applicant has amended claims 1 and 9. Claims 1-9, 11-32, 34 and 35 remain pending.

Claim Rejection Under 35 U.S.C. § 103

In the Final Office Action, the Examiner rejected claims 1-9, 11-33, 34-35 under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). Applicant respectfully traverses the rejection. The applied references fail to disclose or suggest the inventions defined by Applicant's claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention. Before addressing the individual claim rejections, it appears that a brief summary of the prior art is appropriate.

Mathur (USPN 6,424,658)

Mathur describes a store-and-forward network switch that uses an embedded dynamic-random-access memory (DRAM) packet memory. In particular, FIG. 2 of Mathur shows a network switch chip 18 that receives packets from one of four ports A, B, C, D and stores the packets in embedded DRAM packet memory 20. The network switch chip 18 transmits the stored packets out to one or more of the four ports A, B, C, D. The following illustrates FIG. 2 of Mathur:

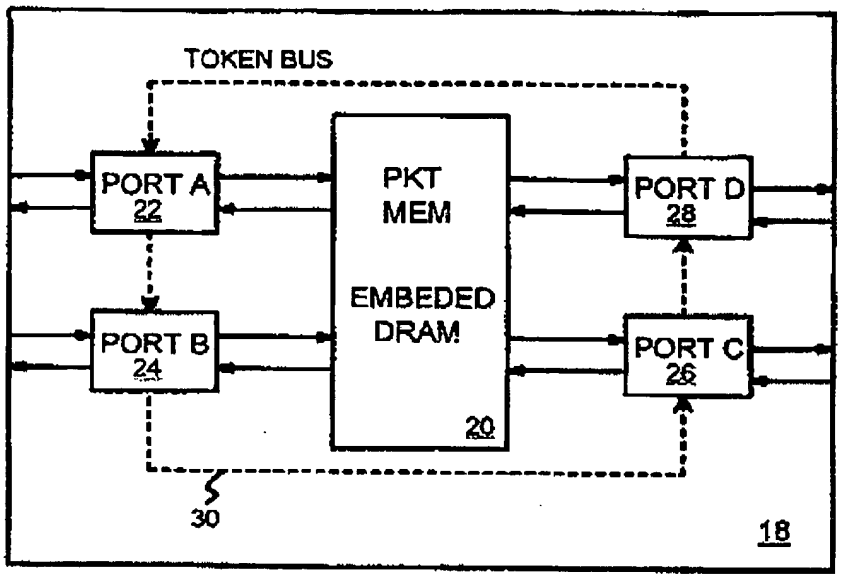

FIG. 2

Mathur makes clear that packets forwarded in any direction between ports 22-28 are stored in embedded packet memory 20. For example, at col. 6, ll. 3-7, Mathur specifically states the following:

> *Port logic 22, 24, 26, 28 are bi-directional ports to a network node connected to a computer, peripheral, LAN segment, or other network equipment such as another switch, router, repeater, bridge or hub. Packets may be input or output from any port. When a packet is received by port logic 22, 24, 26, 28, it first writes the packet into embedded DRAM packet memory 20.*

Thus, as stated above and illustrated in FIG. 2 (above), Mathur teaches a switch in which packets forwarded between any of the four interface ports 22-26 are buffered within an embedded packet memory 20 regardless of the forwarding direction.

Muller et al. (USPN 6,246,680)

Muller describes a highly integrated multi-layer switch element. According to Muller, the switch element includes multiple ports for transmitting and receiving packets over a network. FIG. 2 of Muller illustrates the described switch element:

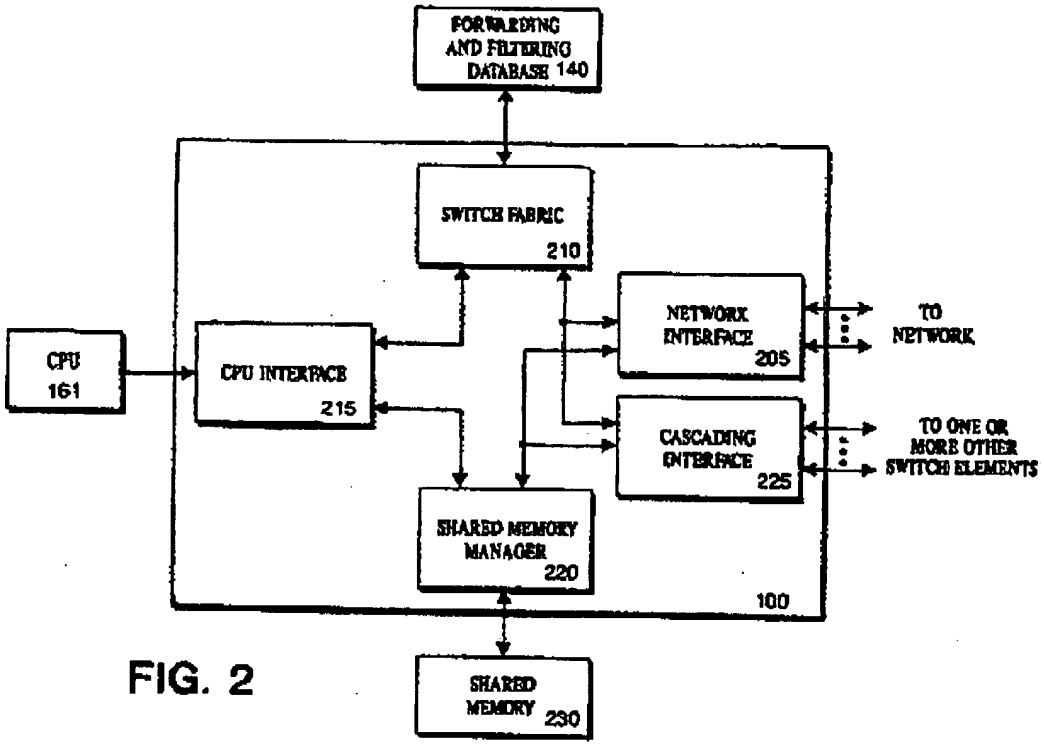

FIG. 2

Unlike Mathur, Muller makes use of an external shared memory 230 for buffering packets flowing between any of the network interfaces 205. For example, col. 1, ll. 41-60 of Muller states:

> *Input packet processing includes the following: (1) receiving and verifying incoming Ethernet packets, (2) modifying packet headers when appropriate, (3) requesting buffer pointers from the shared memory manager 220 for storage of incoming packets, (4) requesting forwarding decisions from the switch fabric block 210, (5)* ***transferring the incoming packet data to the shared memory manager 220 for temporary storage in an external shared memory 230,*** *and (5) upon receipt of a forwarding decision, forwarding the buffer pointer(s) to the output port(s) indicated by the forwarding decision. Output packet processing may be performed by one or more output ports of the network interface 205. Output processing includes* ***requesting packet data from the shared memory manager 220,*** *transmitting packets onto the network, and requesting deallocation of buffer(s) after packets have been transmitted.*

Thus, Muller teaches a switch in which an external shared memory 230 is used to buffer packets flowing in between network interfaces 205 regardless of direction.

Claims 1, 4-8

Unlike the teachings of either Mathur or Muller, Applicants' claim 1 is directed to a routing component that buffers data forwarded between two interfaces differently based on the direction the data flows. In particular, claim 1 requires that data forwarded in one direction is buffered differently from data forwarded in an opposite direction between the same interfaces. In other words, Applicant's claim 1 requires that different buffering techniques are used for data flowing between the same two interfaces depending upon the direction of the date.

Neither Mathur nor Muller, either singularly or in combination, teach or suggest utilization of different buffering techniques between the same interfaces depending on the direction of the data flow. As described above, Mathur specifically teaches the use of an embedded memory for buffering all data regardless of direction. Muller teaches use of a shared memory for buffering data regardless of direction. Thus, neither Mathur nor Muller, either singularly or in combination, provide a suggestion of a routing component that utilizes different buffering techniques between the same two network interfaces depending on the direction of the data flow, as required by claim 1.

For example, Applicants' claim 1 requires a routing component that includes an embedded memory within an integrated circuit to buffer data communicated in a first direction from a first interface to a second interface, and a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface to the first interface. Again, Mathur in view Muller, does not provide one skilled in the art with a teaching or suggestion to utilize different buffering techniques between the same two network interfaces depending on the direction of the data flow between those two interfaces.

The practicality of this non-obvious technique is set forth in the present application. For example, pg. 6, ll. 8-16 of the present application states:

> In the scalable router arrangement, data communicated from a faster interface to a slower interface is stored in an external memory associated with the routing component that received the data. Thus, for example, data received via the crossbar arrangement is buffered in the

> external memory before being output via a WAN interface. Data communicated from the WAN interface to the crossbar arrangement [i.e., the opposite direction], on the other hand, is stored in an embedded memory device. ...

Thus, as illustrated by this example, the described routing architecture may utilize an internal embedded memory when forwarding data from a slower interface (e.g., a WAN interface) to a faster interface (e.g., a switch fabric). However, the same routing component may use an external memory when forwarding data in an opposite direction from the faster interface to the slower interface. This architecture may have certain advantages. For example, pins that may otherwise be used for buffering traffic in a lower bandwidth direction may be avoided, and additional pins may instead be used to allow utilization of larger external memory for buffering traffic flowing between the same interfaces but in a higher bandwidth direction.

Quite contrary to this approach, both Mathur and Muller teach utilization of the same buffering scheme regardless of the direction of the packet flow. In the case of Mathur, an embedded memory is used for all directions. In the case of Mathur, a shared memory is used for all directions. Even when viewed in combination, the references fail to provide a teaching or suggestion of a routing component that utilizes different buffering schemes when forwarding packets in opposite directions between the same two interfaces, as required by claim 1.

In rejecting claim 1, the Examiner essentially argues that it would be obvious to one skilled in the art to replace the embedded memory of Mathur with the shared memory of Muller. However, the Examiner incorrectly concludes that one of ordinary skilled would have ascertained from Mathur and Muller the utilization of different buffering schemes between two interfaces based on direction. In particular, the Examiner concludes that one of ordinary skilled would have ascertained from Mathur and Muller to utilize an embedded memory to buffer packets flowing between two interfaces in a first direction, yet utilize an external memory when buffering packets flowing between the same two interfaces in the opposite direction. These conclusions are not based on evidence of record. Nowhere do Mathur or Muller, either singularly or in combination, teach or suggest use of embedded and external memories in the manner claimed by the Applicant.

Moreover, Applicant disagrees that Mathur or Muller provide any motivation for the modifications proposed by the Examiner. The Examiner argument is that Muller provides such a motivation by stating that the shared memory system achieves "efficient allocation ... that is

proportional to the amount of traffic through a given port." However, this statement of Muller refers to memory allocation. Specifically, Muller is merely stating that memory allocation within the external shared memory is dynamic and based on the amount of traffic through a given port. This does not provide a suggestion to modify the architecture of the Mathur switch to utilize embedded memory for only one direction while using an external memory for data flowing between the same interfaces in the opposite direction. This statement only suggests that the amount of shared memory allocation may dynamically vary based on traffic levels, not that the different memory architectures are used. Unlike Mathur's shared memory approach, Applicants' system does not require dynamically memory allocation based on traffic levels, and the statements of Mathur relied upon by the Examiner do not provide motivation for Applicants' claimed invention.

Further, the modification to Muller as proposed by the Examiner is directly contrary to the express statements of Muller. Muller clearly states that the use of embedded memory avoids numerous problems associated with external memories. For example, at col. 12, ll. 25-65, Muller specifically denounces the use of external memories due to increased pin counts, slow access times and limited memory depth:

> *A network switch with shared embedded DRAM is ideally suited for higher network speeds such as 100 Mbps, 1 Gbps and beyond. Ports can be added without significantly increasing the cost of the switch. The network switch can support a large number of high-speed ports. Increasingly larger numbers of pins for external memory access on a network-switch chip are avoided as higher network speeds are used and higher memory bandwidth is required. A high memory-bandwidth network switch uses a store-and-forward memory with sufficient memory bandwidth for 1 Gbps networks.*
>
> *Memory access times have been decreasing at a slower pace than the increase in Ethernet speeds. Higher bandwidth is achieved with the embedded packet memory by increasing the bus width to the memory.*
>
> ***Using the embedded memory eliminates the pincount problem**, since the wider memory bus is entirely internal to a semiconductor integrated circuit chip. Memory bandwidth can be increased by increasing the width of the internal bus without increasing a number of external I/O pins on the IC package. A 256-bit-wide internal DRAM produces a bandwidth in excess of 3 Gbytes/sec. This is a sufficiently large bandwidth to achieve a 128-port 100 Mbps network switch or a 12-port 1-Gbps switch.*
>
> ***Using a DRAM embedded memory rather than an external SRAM memory greatly increases the available memory depth.***

Thus, Muller makes clear that the use of external memory is undesirable. Moreover, even if the Examiner's arguments were assumed true that one skilled in the art would for some reason be

motivated to replace the embedded memory of Muller with an external memory, why would he or she only utilize the external memory for a single direction? Assuming the Examiner's reasoning is correct, based on the teaching of Muller and Mathur, would not a person of ordinary skill then modify Muller to utilize shared memory in both directions? The Examiner has offered no explanation as to how one of ordinary skill in the art would achieve Applicant's claimed invention when both Muller and Mathur employ switches that utilize the same buffering techniques regardless of direction of packet forwarding.

In summary, Muller in view of Mathur fails to teach or suggest specific elements of Applicant's claims (e.g., use of different buffering techniques between the same interfaces based on forwarding direction), and provide no motivation to achieve a routing component as claimed by the Applicants.

With regard to claims 4 and 5, Muller in view of Mathur fails to teach or suggest a routing component that utilizes an embedded memory to buffer data received from a wide area network (WAN) and forwarded to a switch fabric, and that utilizes an external memory to buffer data received from the switch fabric and forwarded in the opposite direction to the WAN. Again, contrary to these requirements, both Muller and Mathur teach using the same type of buffering scheme for all directions. The Examiner has failed to cite a reference in which the buffering technique is different between the same two interfaces (i.e., a WAN and a switch fabric) based on the forwarding direction, as required by Applicants' claims 4 and 5.

Claims 6-8 depend from claim 1 and are allowable for at least the reasons the reasons set forth above.

Claims 9, 11-17

Independent claim 9 is directed to a network element having a first network interface, a second network interface, and a routing component formed in an integrated circuit. Claim 9 further requires that the routing component buffers data in the embedded memory that is communicated in a first direction from the first network interface to the second network interface, and wherein the routing component buffers data in the second memory that is communicated in a second direction from the second network interface to the first network interface.

For reasons set forth above, Mathur in view of Muller fails to teach or suggest a network element that buffers data forwarded between two interfaces in one direction using an embedded memory and buffers data forwarded in an opposite direction between the same interfaces using an external memory, as required by Applicants' claim 9.

Similarly, Mathur in view of Muller fails to teach or suggest a routing component that utilizes an embedded memory to buffer data communicated in a first direction from a WAN to a switch fabric, and utilizes an external memory for buffering data communicated in a second direction from the switch fabric to the WAN, as generally required by claims 12 and 13, respectively.

Claims 14, 16, 17 depend from claim 9 and are allowable for at least the reasons states above.

Claims 18-29

For reasons set forth above, Mathur in view of Muller fails to teach or suggest teach or suggest an integrated circuit that comprises an embedded memory to buffer data communicated in a first direction from a first interface to the second interface, and an interface to a memory external to the IC for buffering data communicated in a second direction from the second interface to the first interface, as required by independent claims 18 and 24.

With respect to claims 26 and 27, for at least the reasons stated above, neither Mathur in view of Muller teach or suggest an integrated circuit having an embedded memory to buffer data communicated in a first direction from a wide area network (WAN) to a switch fabric, and an interface to utilize an external memory for buffering data communicated in an opposite direction from the switch fabric to the WAN.

Claims 30-32, 34

Mathur in view of Muller fails to teach or suggest teach or suggest utilization of a different buffering architecture with respect to internal and external memory based on the different direction that packets are forwarded between the same two interfaces. For at least this reason, Mathur in view of Muller fails to teach or suggest the requirements of amended claim 30.

With respect to claim 32, for at least the reasons stated above, Mathur in view of Muller fails to teach or suggest: receiving inbound data from wide area network (WAN) via a first routing component; buffering the inbound data within an embedded memory internal to the first routing component; forwarding the inbound data from the first routing component to a second routing component via a switch; receiving outbound data with the first routing component from the switch; buffering the outbound data within a memory external to the first routing component; and forwarding the outbound data to the network first interface.

Claim 35

Similarly, with respect to claim 35, Mathur in view of Muller fails to teach or suggest teach or suggest utilization of a different buffering architecture with respect to embedded and external memory based on the different direction that packets are forwarded between the same two interfaces.

For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicants' claims 2, 3, 10, 11, and 18-35 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date: August 31, 2005

By: Mark J. Sieffert

SHUMAKER & SIEFFERT, P.A.
8425 Seasons Parkway, Suite 105
St. Paul, Minnesota 55125
Telephone: 651.735.1100
Facsimile: 651.735.1102

Name: Kent J. Sieffert
Reg. No.: 41,312